[00013] Operational amplifier circuit 12 includes ~~an operational~~a first amplifier 20 (OA1) having an inverting input 22, a non-inverting input 24 and an output 26. A source of signal current is provided by a sensor element, such as for example, photodiode 28 (D1) which generates current I_s.

[00014] Coupled to output 26 of ~~operational~~ first amplifier 20 is a first voltage divider circuit, generally identified by the numeral 30. ~~Voltage~~ First voltage divider circuit 30 includes a resistor 32 (R1) and a resistor 34 (R2) and has an output 36.

[00015] A first MOS resistor device, generally identified by the numeral 40 (MN1) is coupled between the output 36 of first voltage divider circuit 30 and the inverting input 22 of ~~operational~~ first amplifier 20. First MOS resistor device 40 includes a drain terminal 42, source terminal 44 and gate terminal 46. The gate bias V_g is modulated by the output voltage of ~~operational~~ first amplifier 20 utilizing gate bias circuit 14.

[00016] Gate bias circuit 14 includes ~~an operational~~a second amplifier 60 (OA2) having an inverting input 62, a non-inverting input 64 and an output 66. Output 66 of ~~operational~~ second amplifier 60 is coupled to gate 46 of first MOS resistor device 40.

[00017] Coupled to the output 26 of ~~operational~~ first amplifier 20 is a second voltage divider circuit, generally identified by the numeral 70. Second ~~Voltage~~ voltage divider circuit 70 includes a resistor 72 (R3) and resistor 74 (R4). The output 76 of second voltage divider circuit 70, Vd, is coupled to the inverting input 62 of ~~operational~~ second amplifier 60.

[00018] Also coupled to the output 26 of ~~operational~~ first amplifier 20 is a third voltage divider circuit, generally identified by the numeral 78. Third ~~Voltage~~ voltage divider circuit 78 includes a second MOS resistor device (MN2), generally identified by the numeral 80. Second MOS resistor device 80 includes a drain terminal 82, source terminal 84 and a gate terminal 86. Coupled to the drain terminal 82 of second MOS resistor device 80 is a resistor 88 (R_{ref}). The output of ~~operational~~ second amplifier 60 is applied to the gate terminal 86 of second MOS resistor device 80. The output of third voltage divider circuit 78 is applied to the non-inverting input 64 of ~~operational~~ second amplifier 60. A current source (I_{os}) 90 is also applied to the non-inverting input 64 of ~~operational~~ second amplifier 60.